

FIG. 1
CONVENTIONAL ART

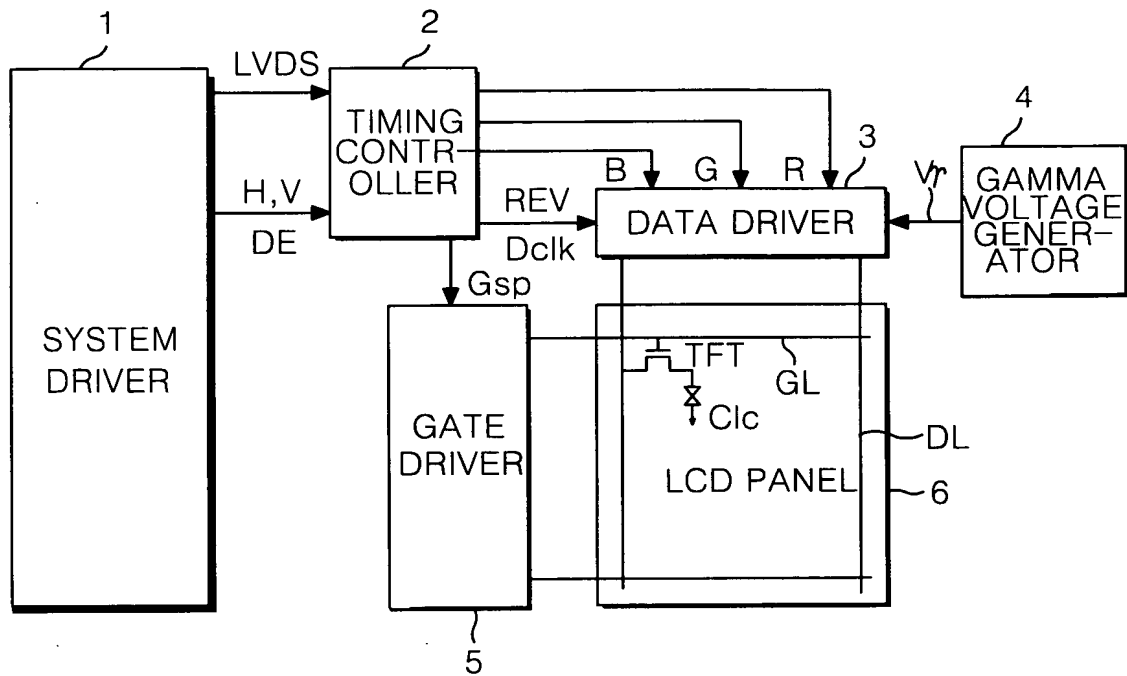


FIG.2
CONVENTIONAL ART

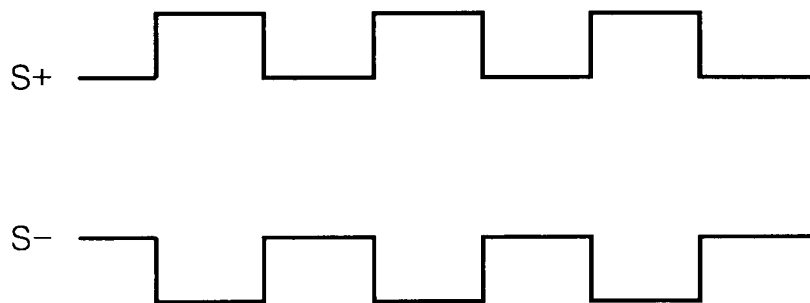
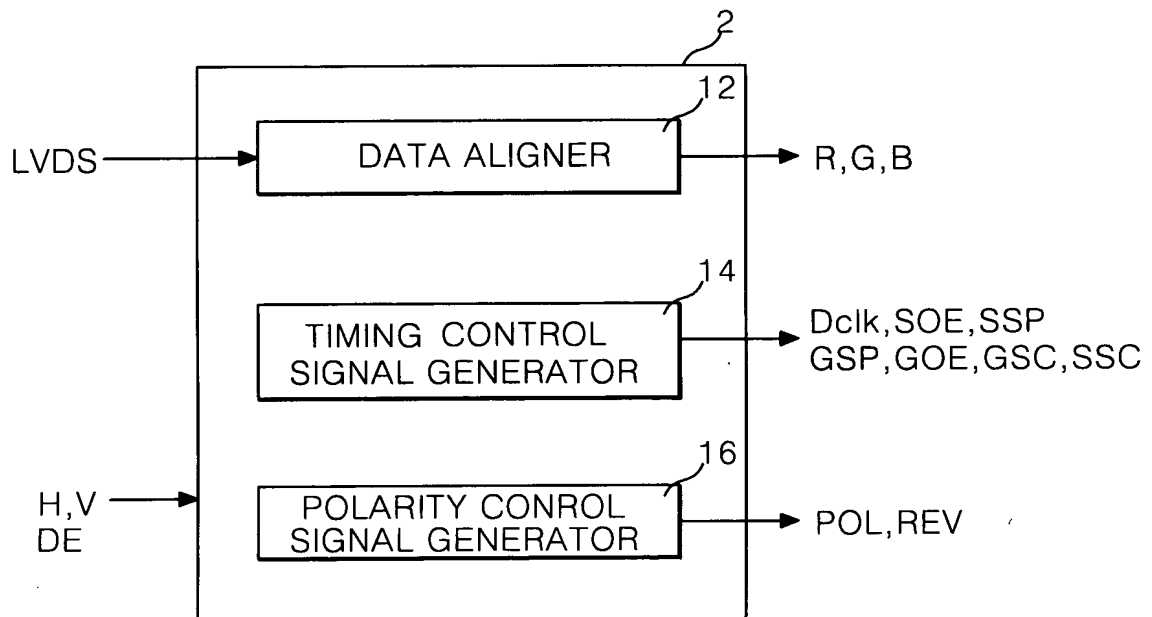


FIG.3
CONVENTIONAL ART



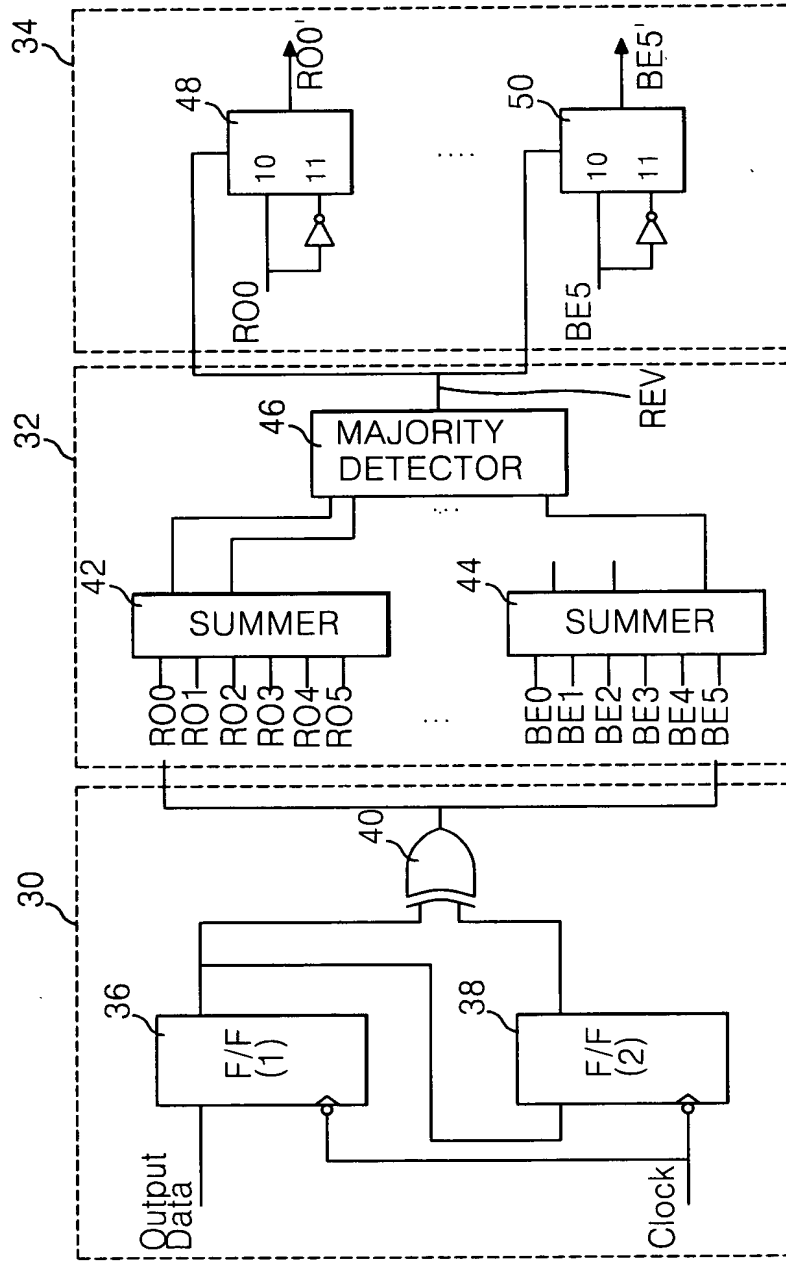
[illegible]

FIG. 4B
CONVENTIONAL ART

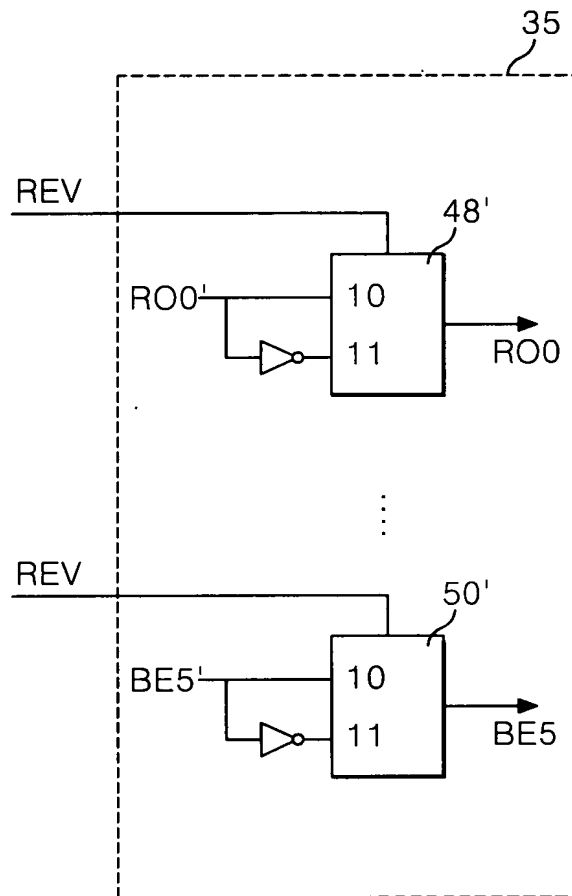


FIG.5
CONVENTIONAL ART

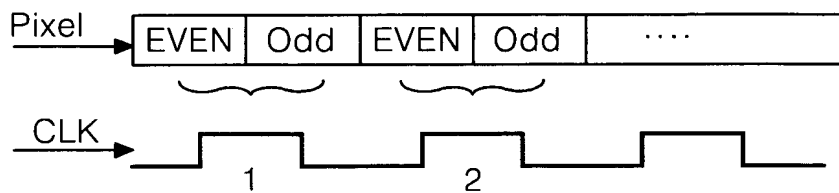


FIG. 6

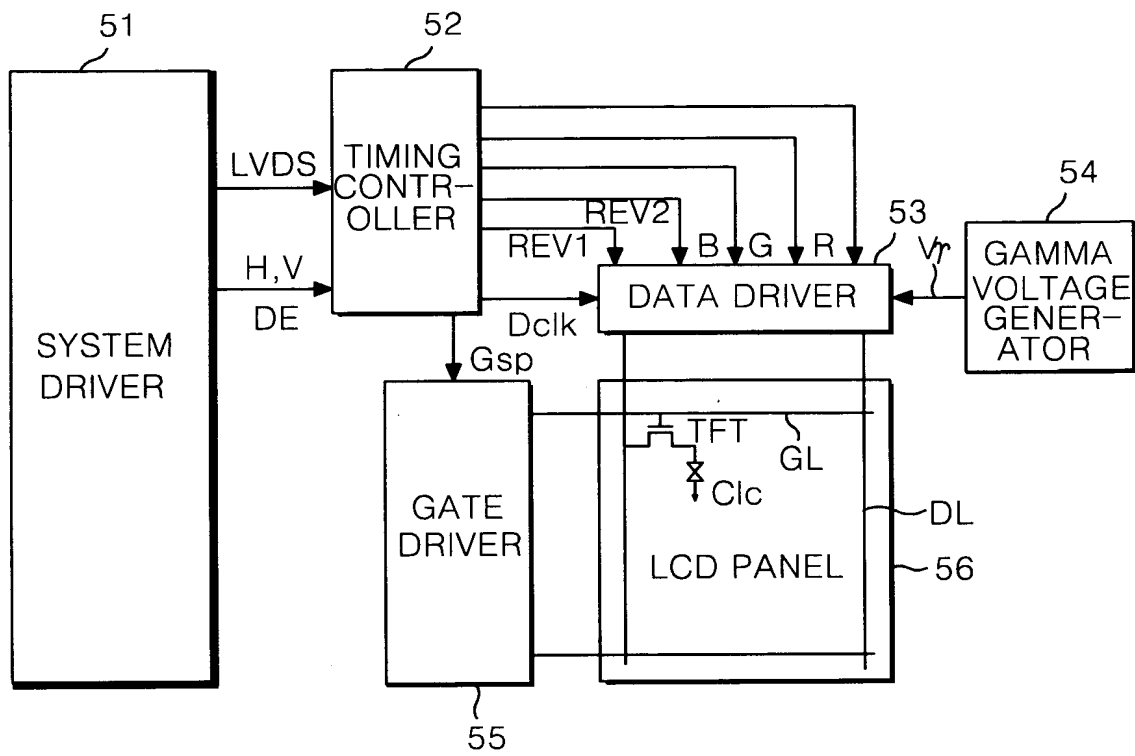


FIG. 7

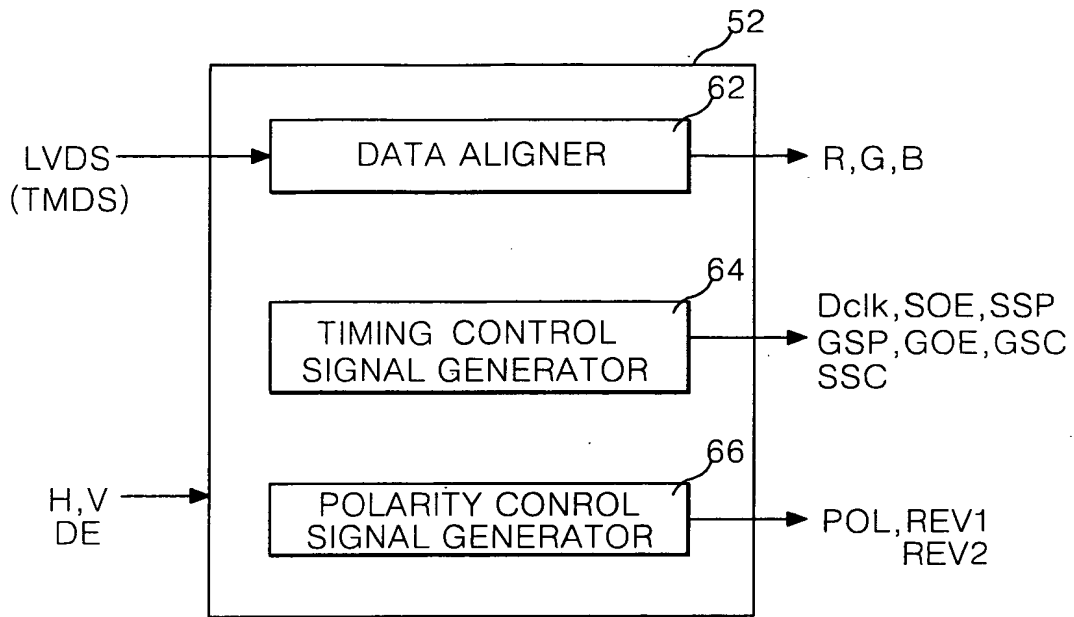


FIG. 8A

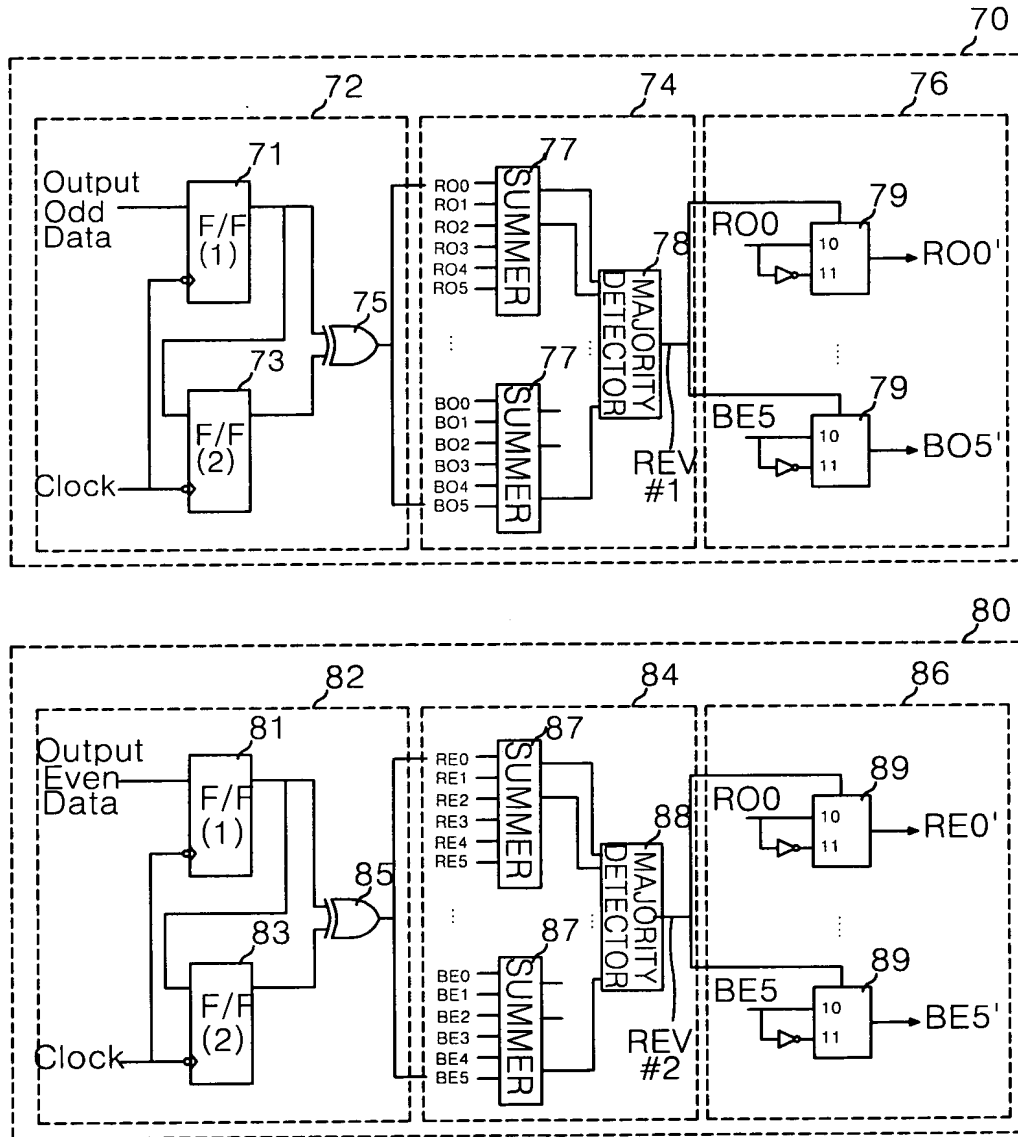


FIG. 8B

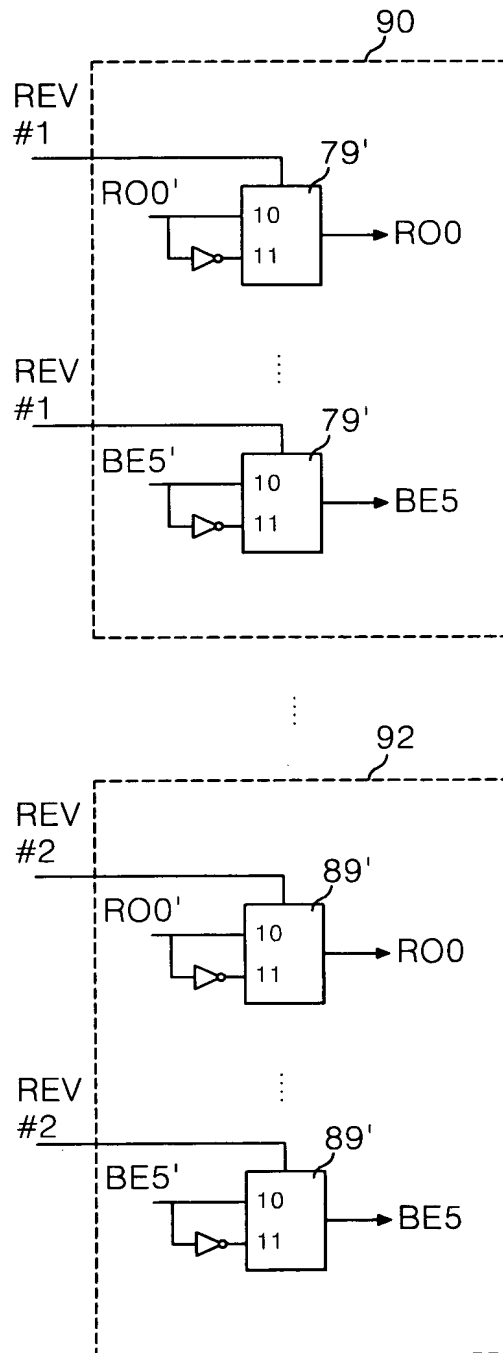


FIG.9

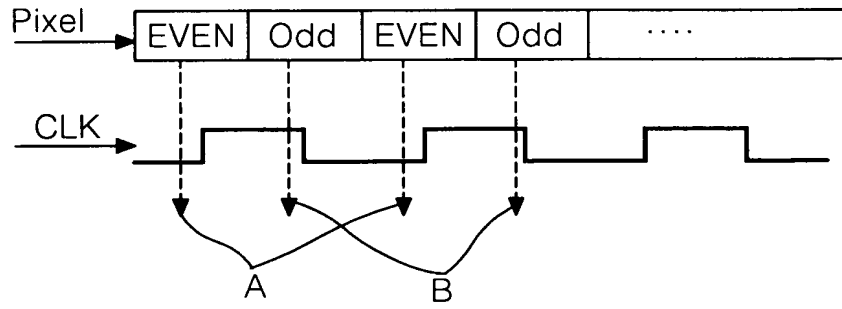


FIG. 9 is a timing diagram showing the relationship between the Pixel and CLK signals. The Pixel signal is a sequence of data elements (EVEN, Odd, EVEN, Odd, ...). The CLK signal is a periodic square wave. The diagram illustrates the timing relationship between the Pixel and CLK signals, showing that the Pixel signal is sampled at the rising and falling edges of the CLK signal. The EVEN pixels are sampled at the rising edge (A), and the Odd pixels are sampled at the falling edge (B).

FIG. 10

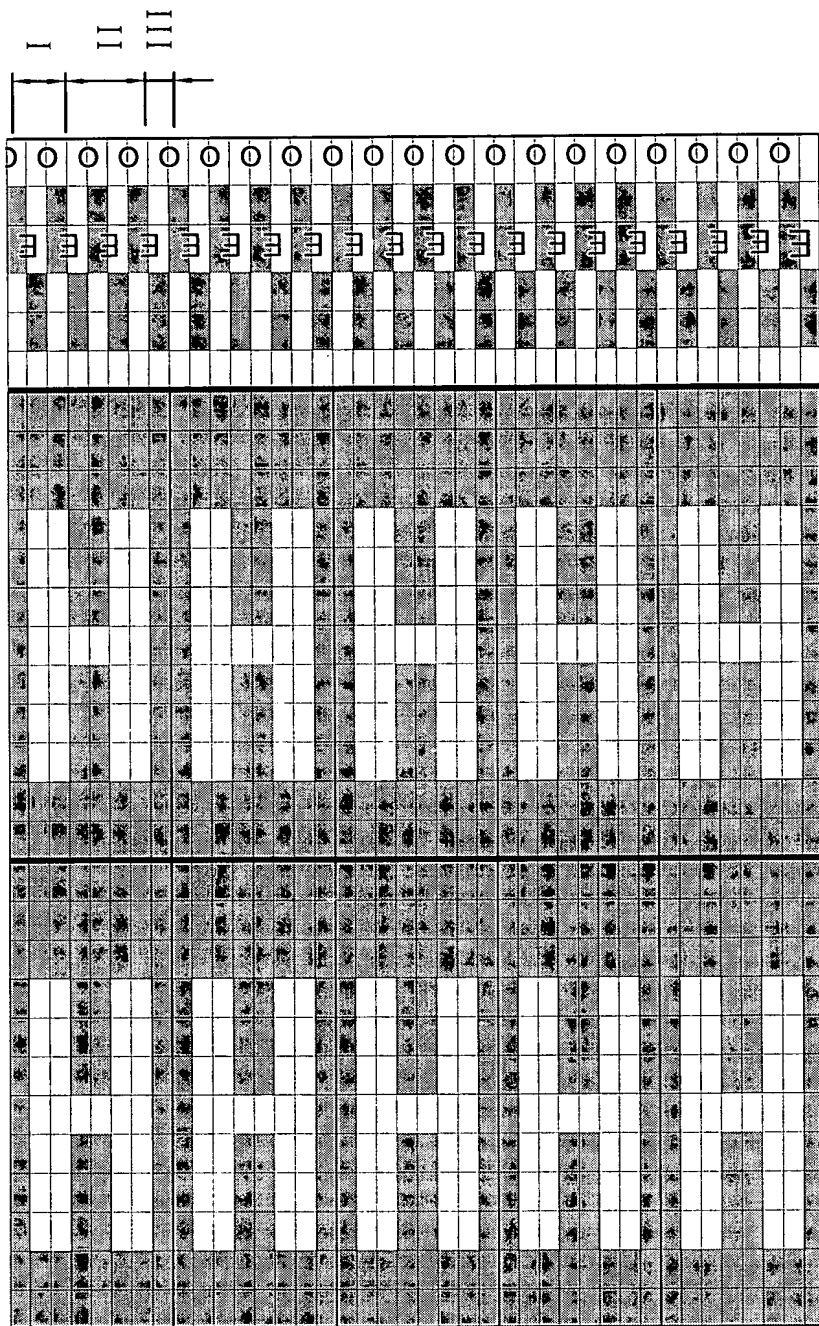


FIG.11

	Dn	Dn-1	Dn-2	Dn-3	Dn-4	Dn-5	Dn-6	Dn-7	Dn-8
RE0	1	0	0	0	1	0	0	0	1
RE1	1	0	0	0	1	0	0	0	1
RE2	1	0	0	0	1	0	0	0	1
RE3	1	0	0	0	1	0	0	0	1
RE4	1	0	0	0	1	0	0	0	1
RE5	1	0	0	0	1	0	0	0	1
GE0	1	0	0	0	1	0	0	0	1
GE1	1	0	0	0	1	0	0	0	1
GE2	1	0	0	0	1	0	0	0	1
GE3	1	0	0	0	1	0	0	0	1
GE4	1	0	0	0	1	0	0	0	1
GE5	1	0	0	0	1	0	0	0	1
BE0	1	0	0	0	1	0	0	0	1
BE1	1	0	0	0	1	0	0	0	1
BE2	1	0	0	0	1	0	0	0	1
BE3	1	0	0	0	1	0	0	0	1
BE4	1	0	0	0	1	0	0	0	1
BE5	1	0	0	0	1	0	0	0	1
RO0	0	0	0	1	0	0	0	1	0
RO1	0	0	0	1	0	0	0	1	0
RO2	0	0	0	1	0	0	0	1	0
RO3	0	0	0	1	0	0	0	1	0
RO4	0	0	0	1	0	0	0	1	0
RO5	0	0	0	1	0	0	0	1	0
GO0	0	0	0	1	0	0	0	1	0
GO1	0	0	0	1	0	0	0	1	0
GO2	0	0	0	1	0	0	0	1	0
GO3	0	0	0	1	0	0	0	1	0
GO4	0	0	0	1	0	0	0	1	0
GO5	0	0	0	1	0	0	0	1	0
BO0	0	0	0	1	0	0	0	1	0
BO1	0	0	0	1	0	0	0	1	0
BO2	0	0	0	1	0	0	0	1	0
BO3	0	0	0	1	0	0	0	1	0
BO4	0	0	0	1	0	0	0	1	0
BO5	0	0	0	1	0	0	0	1	0

DATA OUTPUT UPON REV OFF

FIG.12

	Dn	Dn-1	Dn-2	Dn-3	Dn-4	Dn-5	Dn-6	Dn-7	Dn-8
RE0	0	1	1	0	0	1	1	1	1
RE1	0	1	1	0	0	1	1	1	1
RE2	0	1	1	0	0	1	1	1	1
RE3	0	1	1	0	0	1	1	1	1
RE4	0	1	1	0	0	1	1	1	1
RE5	0	1	1	0	0	1	1	1	1
GE0	0	1	1	0	0	1	1	1	1
GE1	0	1	1	0	0	1	1	1	1
GE2	0	1	1	0	0	1	1	1	1
GE3	0	1	1	0	0	1	1	1	1
GE4	0	1	1	0	0	1	1	1	1
GE5	0	1	1	0	0	1	1	1	1
BE0	0	1	1	0	0	1	1	1	1
BE1	0	1	1	0	0	1	1	1	1
BE2	0	1	1	0	0	1	1	1	1
BE3	0	1	1	0	0	1	1	1	1
BE4	0	1	1	0	0	1	1	1	1
BE5	0	1	1	0	0	1	1	1	1
RO0	1	1	1	1	1	1	1	0	0
RO1	1	1	1	1	1	1	1	0	0
RO2	1	1	1	1	1	1	1	0	0
RO3	1	1	1	1	1	1	1	0	0
RO4	1	1	1	1	1	1	1	0	0
RO5	1	1	1	1	1	1	1	0	0
GO0	1	1	1	1	1	1	1	0	0
GO1	1	1	1	1	1	1	1	0	0
GO2	1	1	1	1	1	1	1	0	0
GO3	1	1	1	1	1	1	1	0	0
GO4	1	1	1	1	1	1	1	0	0
GO5	1	1	1	1	1	1	1	0	0
BO0	1	1	1	1	1	1	1	0	0
BO1	1	1	1	1	1	1	1	0	0
BO2	1	1	1	1	1	1	1	0	0
BO3	1	1	1	1	1	1	1	0	0
BO4	1	1	1	1	1	1	1	0	0
	Dn	Dn-1	Dn-2	Dn-3	Dn-4	Dn-5	Dn-6	Dn-7	Dn-8

DATA OUTPUT UPON REV ON

FIG.13

	Dn	Dn-1	Dn-2	Dn-3	Dn-4	Dn-5	Dn-6	Dn-7	Dn-8
RE0	1	1	1	1	1	1	1	1	1
RE1	1	1	1	1	1	1	1	1	1
RE2	1	1	1	1	1	1	1	1	1
RE3	1	1	1	1	1	1	1	1	1
RE4	1	1	1	1	1	1	1	1	1
RE5	1	1	1	1	1	1	1	1	1
GE0	1	1	1	1	1	1	1	1	1
GE1	1	1	1	1	1	1	1	1	1
GE2	1	1	1	1	1	1	1	1	1
GE3	1	1	1	1	1	1	1	1	1
GE4	1	1	1	1	1	1	1	1	1
GE5	1	1	1	1	1	1	1	1	1
BE0	1	1	1	1	1	1	1	1	1
BE1	1	1	1	1	1	1	1	1	1
BE2	1	1	1	1	1	1	1	1	1
BE3	1	1	1	1	1	1	1	1	1
BE4	1	1	1	1	1	1	1	1	1
BE5	1	1	1	1	1	1	1	1	1
RO0	0	0	0	0	0	0	0	0	0
RO1	0	0	0	0	0	0	0	0	0
RO2	0	0	0	0	0	0	0	0	0
RO3	0	0	0	0	0	0	0	0	0
RO4	0	0	0	0	0	0	0	0	0
RO5	0	0	0	0	0	0	0	0	0
GO0	0	0	0	0	0	0	0	0	0
GO1	0	0	0	0	0	0	0	0	0
GO2	0	0	0	0	0	0	0	0	0
GO3	0	0	0	0	0	0	0	0	0
GO4	0	0	0	0	0	0	0	0	0
GO5	0	0	0	0	0	0	0	0	0
BO0	0	0	0	0	0	0	0	0	0
BO1	0	0	0	0	0	0	0	0	0
BO2	0	0	0	0	0	0	0	0	0
BO3	0	0	0	0	0	0	0	0	0
BO4	0	0	0	0	0	0	0	0	0
BO5	0	0	0	0	0	0	0	0	0

DATA OUTPUT UPON REV 1,2 DRIVING (DC LEVEL)

FIG. 14A

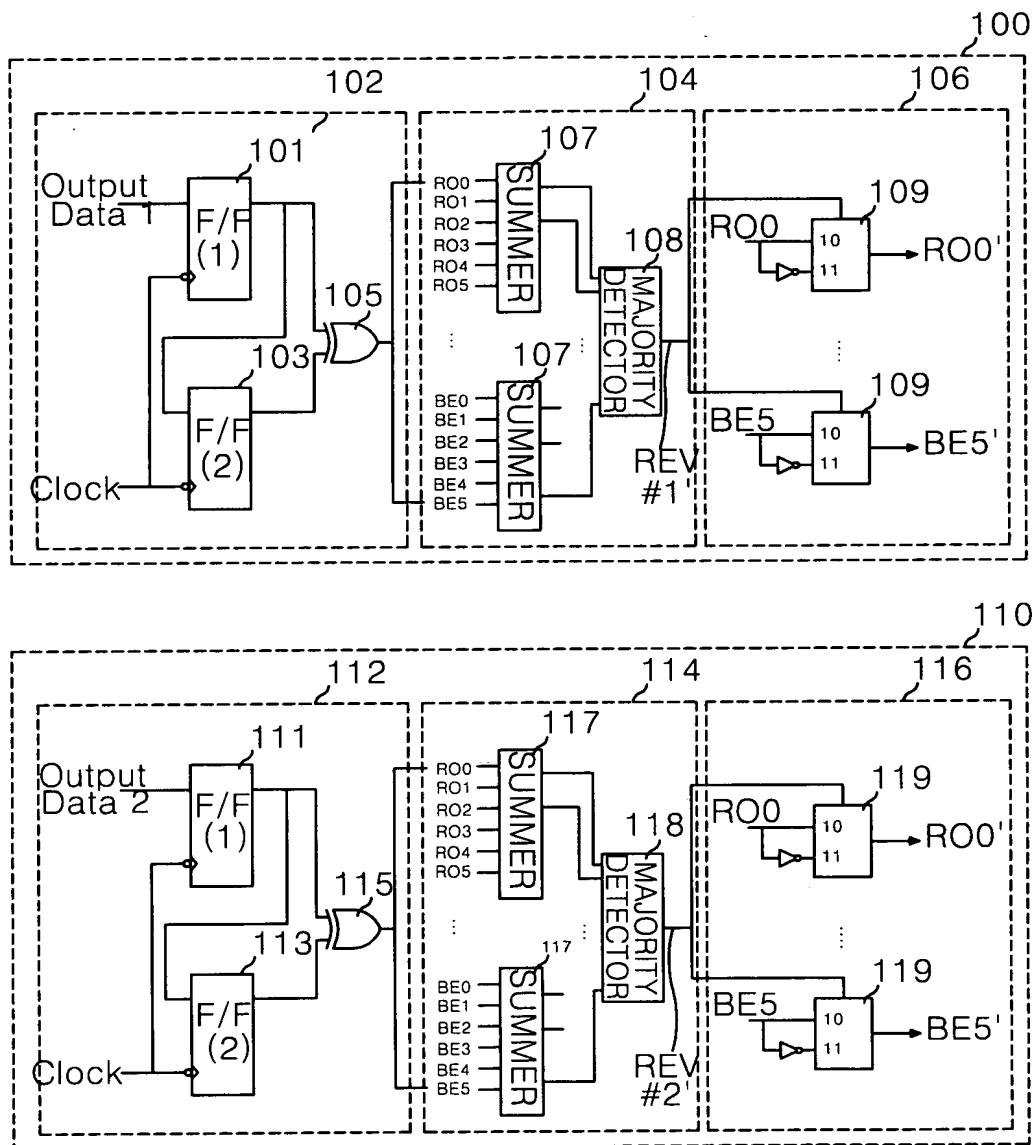


FIG. 14B

